

A-5 LEVEL INVERTER FOR DC GENERATOR REGULATED POWER SUPPLY

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ABSTRACT: 5-level inverters are typically used to convert DC voltage to alternating current voltage. The load can only create two output voltages from the 5-level inverter or converter: +2Vdc and -2Vdc. To generate the AC output voltage, the controller basically swaps two voltages. As a result, this strategy of lowering THD is effective. The use of a high frequency rating has various limits in high-power and high-voltage applications, primarily due to switching loss or device rating restrictions. The 5-Level Inverter idea provides an alternating current signal that is independent of voltage levels. Alternatively, increasingly higher voltage levels are supplied to provide a smoother stepped waveform. This needs the addition of switches to the inverter in order to raise the voltage level and lower the dv/dt. The output waveform becomes smoother as more voltage levels are present. More switches and components are added to the system as we move up the design hierarchy, necessitating a more complex inverter controller.

Keywords: *H-bridge Five level Inverter, THD, Matlab/Simulink.*

1. INTRODUCTION

Power electronics inverters are becoming more and more common in applications involving industrial drives. The advantages of the H-bridge five level inverter in applications requiring high voltage and high power with minimal harmonics have drawn a lot of attention in recent years. The increased harmonic distortion in a typical inverter results in a shorter machine life and a grid voltage synchronization issue. In order to lower the harmonic distortion in a traditional inverter, a big filter that adds bulk to the system is required. We have therefore developed a family of multilevel inverters that can operate at high voltage levels and minimal harmonic distortion in order to reduce the size of the inverter.

2. LITERATURE SURVEY

Numerous studies have demonstrated how traditional inverters, which have higher harmonic

content, can lessen overall harmonic distortion issues by using DC renewable energy sources like solar and wind power systems.

As said by Md. Linton Hossain and Zulkifilie bin Ibrahim In 2014. It is possible to lessen harmonic distortion by utilizing an appropriate topology and control strategy. We talked about a variety of multilevel inverter designs to lower harmonics and enhance voltage quality. The diode clamped, capacitor clamped, and H-bridge type inverter topologies are the most widely utilized ones. If the level increases in the capacitor and diode clamped inverter, the component also increases, making the system cumbersome and challenging to operate. Cascade H-bridge multilevel inverter topology, which is free from capacitor and diode clamping, can be used to fix the issue. The five level cascade H-bridge inverter, which has a straightforward circuit and produces greater output, is the subject of our paper's modeling.

In MLN Vital, P. Yoganand Reddy (2016). Every phase of a single phase multilevel inverter is coupled to a single DC source. Three voltages are produced by each level: positive, negative, and zero. By connecting the AC source to the DC output and utilizing various combinations of the four switches, this can be achieved. When two switches are in the opposite position and are both ON, the inverter will also be ON. When every inverter is turned ON or off, it will turn off. The definition and application of switching angles reduces the total harmonic. Two H bridge inverters are cascading in level 5 of the H bridge inverter. Unlike a traditional multilevel inverter, which has four switches to control the output voltage, this one has five output levels and eight switch devices.

The idea behind this inverter, as described in Vinayaka B.C. & S. Nagendra Prasad, 2014, is to provide a sinusoidal voltage output by series linking five-level H-bridge inverters. The total voltage produced by all of the cells makes up the output voltage. H-bridge, or single-phase full-bridge, inverter. By using various combinations of the four switches, S1, S2, S3, and S4, to connect the dc source to the ac output, the inverter level produces three distinct voltage outputs: +Vdc, 0Vdc, and -Vdc. Switches S 1 and S 2 are activated to produce +Vdc, whereas switches S 3 and S4 are activated to produce -Vdc. The output voltage is zero when the S1 and S2 or S3 and S4 switches are turned. Switches S 7 and S 8 are activated for -Vdc, while S5 and S6 are the same for +Vdc. Each full-bridge inverter level's AC outputs are coupled in a cascade fashion so that the voltage waveform is the total of the outputs. The total voltage produced by all of the cells makes up the output voltage. Given a cell count of n , there are $2n+1$ output voltage levels. One can select the switching angles so as to minimize the overall harmonic distortion. Two($n-1$) switching devices are required for a n level cascaded H bridge multilevel inverter, where n is the number of the output voltage level.

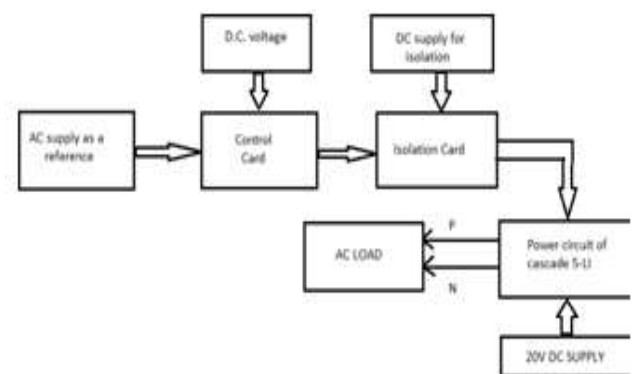
In Chandni M. Vora, Vipul J. Anghan, Purvi B. Anghan, and Archan B. Patel, 2015. The cascaded multilevel inverter, also known as the series h-bridge inverter, is one of the controls used

in multilevel inverters. With this topology, voltage balancing capacitors and clamping diodes are avoided. The cascaded multilevel inverter uses a distinct DC sources design to prevent short circuits of the DC sources. The nature of the individual DC sources makes the series multilevel inverter ideal for a variety of renewable energy sources, including fuel cells and solar cells. The series multi level inverter is the most appropriate for active power conversion, first from AC to DC and then from DC to AC as needed. In high power applications, the cascaded multilevel inverter excels due to its flexibility and adaptability. The suggested topology of multilevel inverters has advantages over alternative topologies, including fewer switches, easier control, and the ability to optimize layout due to the same construction for all levels. Many issues have been encountered when employing h-bridge inverters, and these issues can be resolved by cascading the inverters.

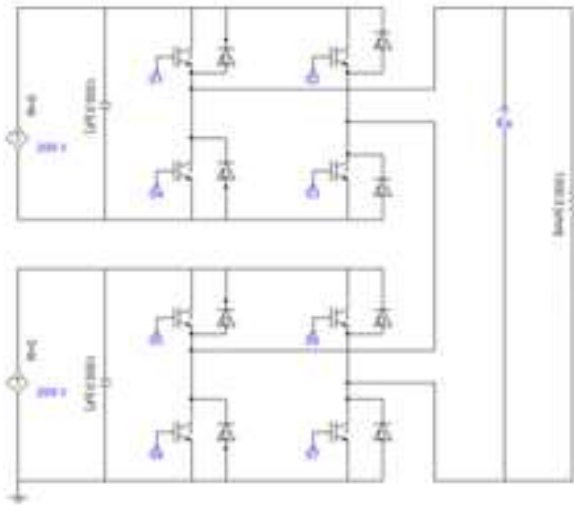
3. MATERIAL AND METHOD

A few things to keep in mind after reading these papers include reduced harmonic distortion and the switch management strategy of the cascading H bridge inverter, which are important for RESs. Therefore, a system that takes into account each of these factors and improves them must be built.

Block diagram



a) Block schematic for a five-level inverter



b) Circuit of control

Control Method

The 5-level inverter's control circuit can regulate the harmonic distortion. The control circuit consists of eight switches that produce three distinct voltage outputs, such as $+V_{dc}$, $0V_{dc}$, and $-V_{dc}$ by using a varied combination of the eight switches ($S_1, S_2, S_3, S_4, S_5, S_6, S_7$, and S_8) to link the DC source to the AC output. The switches S_3, S_4, S_7 , and S_8 are activated when the output voltage reaches zero. Similarly, switches S_1, S_3, S_7 , and S_8 are turned ON when the output voltage is V . While the switches S_1, S_3, S_5 , and S_7 are turned ON when the output voltage reaches $2V$. The switches S_2, S_4, S_7 , and S_8 are turned ON during the $-V$. The switches S_2, S_4 , and S_6 are switched ON while the output voltage is $-V/2$. The switch must be adjusted in order to lower the harmonic and produce the output voltage in this manner, extending the machine's lifespan.

Advantages

It will result in improved waveform quality, which lowers total harmonic distortion and prolongs machine life. Moreover, as the number of switches increases, it will lessen switching stress. The number of sources is twice by the output voltage level. On it, we can also utilize devices with lower voltages.

4. CONCLUSION

Stress across each device decreases as the number of levels increases in terms of %THD and dv/dt . The voltage across each device decreases as the number of switches increases, which reduces switching losses and boosts converter efficiency. One can eliminate the selective harmonics by

adjusting the pulse width. The limit of lowest harmonics can be determined by adjusting the width of pulses, as %THD is dependent on the width of various voltage levels.

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